CLAIMS:

1. A circuit arrangement for controlling a display device (2) which can be operated in a partial mode, comprising a row drive circuit (4) for driving n rows of the display device (2) and a column drive circuit (3) for driving m columns of the display device, wherein the row drive circuit (4) controls the n rows of the display device sequentially from 1 to n, and the column drive circuit (3) supplies column voltages to the m columns, which voltages correspond to the picture data to be displayed of pixels of the controlled row, characterized in that a logic function (L_1-L_n) is included in the row drive circuit (4) in front of at least one row output (Z_1-Z_n), to which logic function a first control signal (R_E) can be supplied, said first control signal (R_E) achieving a deactivation/activation of the row output (Z_1-Z_n) in dependence on the partial mode.

2. A circuit arrangement as claimed in claim 1, characterized in that the logic function (L_1-L_n) is connected in front of each row output (Z_1-Z_n).

3. A circuit arrangement as claimed in claim 1 or 2, characterized in that the logic function (L_1-L_n) is realized as an AND gate.

4. A circuit arrangement as claimed in claim 1, characterized in that the row drive circuit (4) comprises a shift register (41) which has n stages (S_1 to S_n) and n outputs (A_1 to A_n), and in that a second control signal (R_P) can be supplied to the shift register at the input (E) thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs (A_1 to A_n) of the shift register (41) consecutively in dependence on a clock signal (T).

5. A circuit arrangement as claimed in claim 2, characterized in that the second control signal (R_P) is capable of switching off all n row outputs (Z_1 to Z_n) by means of the logic functions (L_1 to L_n) during the control of a line (Z_3, Z_4) that is not to be displayed in the partial mode.

6. A circuit arrangement as claimed in claim 1, characterized in that a control logic (5) in the column drive circuit (3) generates the first control signal (R_E) in dependence on a partial mode and supplies it to the row drive circuit (4).

7. A circuit arrangement as claimed in claim 1, characterized in that the column drive circuit (3) supplies no column voltages to the column outputs (A_1 to A_m) in the case of a line (Z_3, Z_4) that is not to be displayed.

8. A circuit arrangement as claimed in claim 1, characterized in that the frequency of the clock signal (T) can be increased in the case of one or several consecutive rows (Z_3, Z_4) that is or are not to be displayed.

9. A row drive circuit (4) for controlling n rows of a display device (2) having n outputs (A_1 to A_n), with a logic function (L_1 to L_n) connected in front of each row output (Z_1 to Z_n), by means of which function the row outputs (Z_1 to Z_n) can be deactivated/activated in dependence on a partial mode upon the supply of a first control signal (R_E).

10. A display device (2) comprising a circuit arrangement as claimed in any one of the claims 1 to 8.

11. An electronic appliance comprising a display device (2) as claimed in claim 10.

12. A method of realizing a partial mode wherein a display device (2) is controlled by a circuit arrangement comprising a row drive circuit (4) for driving the n rows and a column drive circuit (3) for supplying column voltages, wherein the n rows are sequentially controlled from 1 to n and column voltages necessary for displaying the corresponding picture data of this row are supplied to the m columns, and wherein all row outputs (Z_1 to Z_n) are deactivated by a first control signal (R_E) in the control of a row (Z_3, Z_4) not to be displayed in the realization of a partial mode, while all row outputs (Z_1 to Z_n) are activated again by means of the first control signal (R_E) for the control of a row (Z_1, Z_2, Z_5) that is to be displayed in the partial mode.